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(71) Applicant: MOTOROLA INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: NELSON, David, Paul; 11204 Maplecrest Drive, Huntsville, AL 35803 (US). NABORS, David, Hoy; 1823 Shellbrook Drive, Huntsville, AL 35806 (US).

(74) Agents: WOOD, J., Ray et al.; Motorola Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

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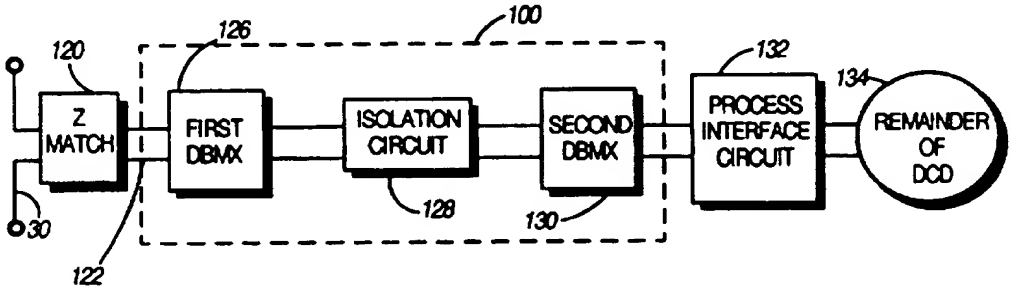

(57) Abstract

An improved isolation circuit for protecting data communications equipment from high voltages on a transmission line has two mixers (124, 130). The first dual balanced mixer (DBMX) (124) translates a data signal on the transmission line (30) to a high frequency and is coupled with an isolation circuit (128) to the second DBMX (130). The second DBMX (130) then translates the output of the first DBMX (124) to an isolated data signal with the same frequency content as the original data signal.

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LINE INTERFACE APPARATUS AND METHOD FOR ISOLATING DATA TERMINAL EQUIPMENT FROM THE LINE

Field of the Invention

This application relates to data communication devices, including, but not limited to, a line interface apparatus and method for isolating data terminal equipment from the line.

Background of the Invention

Data communication devices (DCDs) are used for data communications between terminals or computers over data lines such as dial-up and dedicated telephone lines. These DCDs include modems, terminal adapters, and digital service equipment. DCDs should be isolated from high voltages that may occur on the data lines. Considering the damage that high voltage can cause the low voltage electronics residing in the DCDs, it is necessary to isolate the low voltage electronics from high voltages. This requirement is set forth in equipment specifications such as Underwriters Laboratory 1459 and Bellcore Technical Reference TR-NWT-001089.

The methods currently used for isolation include transformers and high-voltage capacitors. Both these methods are unsatisfactory. Line isolation based on the use of transformers depends on the enamel coating on the magnet wire windings to provide protection. This enamel coating adversely affects the telecommunications signals due to the leakage inductance associated with wire to wire spacing. The transformers used are relatively large and expensive components of the data communications equipment. Because High-voltage capacitors must provide a low impedance to the data signal, they tend to be physically large.

An improved method of isolating DCDs from the data lines that will also reduce size and cost is desirable.

Brief Description of the Drawings

FIG. 1 shows a DCD connected to a transmission line and to a data terminal.

FIG. 2 shows a line interface circuit.

FIG. 3 shows a schematic for a double-balanced mixer.

FIG. 4 shows details of a line interface circuit.

Description of the Preferred Embodiment

In order to provide low cost and efficient isolation, a line interface circuit has a first mixer coupled to the line for receiving the data signal and transforming the data signal to a high frequency data signal. A voltage isolation circuit coupled to the first mixer isolates the high frequency data signal, thereby generating an isolated high frequency data signal. A second mixer coupled to the voltage isolation circuit and the data terminal equipment transforms the isolated high frequency data signal to a low frequency isolated data signal. Electrical components using this improved circuitry typically require approximately 5% less of the volumetric space as conventional methods. In addition, both component cost and manufacturing cost are reduced.

Referring to FIG. 1, a DCD 50 provides an interface between a data terminal equipment (DTE) 40 and the transmission line 30. The DTE 40 may be, but is not limited, to personal computers, computer terminals, switched digital devices, and test equipment. The DTE 40 transfers data to/from the DCD via interface 60 which includes, but is not limited to, RS-232, V.35, and RS422 type interfaces. The DCD 50 includes a line interface circuit (LIC) 100 to interface data signals to the line 30 through an impedance matching network 120 (if required) and data processing circuitry to translate data between the LIC 100 and the DTE interface 60. This configuration provides a communications link between the DTE 40 and the transmission line 30.

As shown in FIG. 2, the LIC 100 connects to an impedance matching network 120 with connection link 122. The impedance matching network 120 connects directly to the transmission line 30. The

LIC 100 comprises a first double-balanced mixer (DBMX) 124 which translates the data signal at connection link 122 to a higher frequency data signal. First DBMX 124 is coupled to Isolation circuit 128 provides high voltage isolation between first DBMX 124 and second DBMX 130 while presenting a low impedance path for the high frequency data signal, thereby generating an isolated high frequency data signal. Second DBMX 130 translates the isolated high frequency data signal to an isolated low frequency data signal. The output of second DBMX 130 is coupled to processor interface circuit 132. The low frequency data signal has approximately the same information and frequency spectrum as the data signal at connection link 122. The process interface circuit (PIC) 130 provides interface between the LIC 100 and the remainder of the DCD 134. The PIC 132 provides a hybrid type interface where the transmit and receive data signals of the DCD are combined to produce signals suitable for transmission on the transmission line. The PIC 132 includes transmit signal conditioning and a receive equalizer for line loss compensation.

The schematic for the first DBMX 124 is shown in FIG. 3. First DBMX 124 includes an intermediate frequency (IF) port 150, a local oscillator (LO) port 152, and a radio frequency (RF) port 154. The IF port 150 is connected to the center taps of RF input transformers 156 and output transformer 158. Transformers 156, 158 are connected together via a diode bridge network 160. The LO port 152 connects to input transformer 156 to provide a high frequency signal to modulate the signal present at the IF port 150. RF port 154 connects to output transformer 158. The first DBMX 124 translates the signal at IF port 150 to a high frequency data signal at the RF port 154 by a frequency amount approximately equal to the input signal frequency present at the LO port 52. The first DBMX 24 also translates an input RF signal to a lower frequency signal at the IF port 150 by a frequency amount essentially equal to the input signal frequency present at the LO port 152. The second DBMX 130 is the same configuration as the first DBMX 124 where the RF port connects to isolation circuit 128 and the IF port connects to processor interface circuit 132, as shown in FIG. 2.

The interface circuit is shown in FIG. 4. The transmission line 30 is connected to the IF port 150 of the first DBMX 124 by means of an impedance matching network 200 including resistors 202, 204, 206. The impedance matching network 200 is used (if necessary) to match the line characteristic impedance to the input impedance of the first DBMX 124. A typical application would require matching a 135 ohm transmission line impedance to a 50 ohms IF port 150 impedance. In such an application, values for resistors 202, 204 would be 107 ohms and the value for resistor 206 would be 63 ohms. In some applications, the LO port 152 to IF port 150 signal leakage may require a filter capacitor 208 across the IF port 150 to attenuate the LO frequency. A typical value for filter capacitor 208 would be 15 nanofarads (nF) for an LO frequency of 10 megahertz (MHz) and an IF input port impedance of 50 ohms, which would present a low impedance at the LO frequency and a 3 decibel frequency of approximately 200 kilohertz (KHz).

The first DBMX 124 of the LIC 100 is driven at the LO port 152 with a 10 MHz oscillator 210. The oscillator 210 couples through a line isolation network 212 which includes capacitors 214, 216. Line isolation network 212 provides high voltage isolation between the oscillator 210 and the LO port 152 of the first DBMX 124. Typical values for capacitors 214, 216 would be 15nF with a voltage withstand rating of 2500 VDC (volts direct current) to provide high voltage isolation with a low impedance (1 ohm) signal path at the LO frequency of 10 MHz. The signal at IF port 150 is translated up in frequency by the oscillator frequency at the LO port 152. The resulting high frequency signal is present at the RF port 154. The high frequency signal at the RF port 154 is also translated down in frequency by the frequency present at the IF port 132.

The isolation circuit 128 couples the high frequency signals between the RF port 154 and the second DMBX RF port 209. The isolation circuit 128 includes capacitors 215, 217 and provides high voltage isolation between the RF ports 154, 209 of the two DBMX's 124, 130. Typical values for capacitors 215, 217 would be 15 nF with a voltage withstand rating of 2500 VDC to provide high voltage isolation

with a low impedance of approximately 1 ohm to the signal path for the carrier frequency of 10 MHz.

The second DBMX 130 has a high frequency signal present at the second DMBX RF port 209. This signal is translated down in frequency by an amount defined by the second DMBX LO port 218 frequency. The second DMBX LO port 218 is also driven by oscillator 210 . Low frequency signals at the second DMBX IF port 220 are also translated up in frequency by the second DMBX LO port 218 frequency and result as high frequency signals at the second DMBX RF port 209. A filter capacitor 222 may be required as a shunt element at the input of PIC 130 to attenuate any leakage signal at the oscillator frequency. A typical value for capacitor 132 would be 15nF, which presents a low impedance across the IF port 124 at an oscillator frequency of 10 MHz and provides an IF 3dB bandwidth of approximately 200KHz for an IF port impedance of 50 ohms.

The PIC 132 in FIG. 4 interfaces the second DBMX IF port 220 to the transmit/receive circuitry 224 of the DCD 50. The PIC 134 includes transmitter conditioning, receiver equalizer, and a hybrid combining network for transmit and receive signal transmission on a single pair line.

By sourcing both DBMX's 124, 130 from a common oscillator 210, the signal from the transmission line connected to the IF port 124 is translated up in frequency, coupled to the second DBMX 106 via the isolation circuit 128, and translated down in frequency to the second DBMX IF port 220 by the same frequency. This process retains the low frequency integrity of the input signal while providing a high voltage isolation barrier between the DBMX's 124, 130. Also, the signal presented at the second DBMX IF port 220 is translated up in frequency, coupled to the first DBMX 124 through isolation circuit 128, and back down in frequency by the same amount in the first DBMX 124. Thus, a low frequency signal is provided for the transmission line at the IF port 150. Low frequency signal integrity is maintained with a high voltage isolation barrier.

Claims

1. A line interface circuit (100) for coupling data terminal equipment to a line, the data terminal equipment receiving a data signal over the line, comprising:

(a) a first mixer (102) coupled to the line for receiving the data signal and transforming the data signal to a high frequency data signal (110);

(b) a voltage isolation circuit (104) coupled to the first mixer for isolating the high frequency data signal, thereby generating an isolated high frequency data signal (112); and,

(c) a second mixer (106) coupled to the voltage isolation circuit and the data terminal equipment for transforming the isolated high frequency data signal to a low frequency isolated data signal (132).

2. The line interface circuit of claim 1, where the voltage isolation circuit comprises high-voltage capacitors connected between the first mixer and the second mixer.

3. The line interface circuit of claim 1, the first mixer being a double-balanced mixer.

4. The line interface circuit of claim 1, the second mixer being a double-balanced mixer.

5. The line interface circuit of claim 1, the low frequency isolated data signal having a frequency spectrum that is almost identical to the frequency spectrum of the data signal .

6. The line interface circuit of claim 1, the first mixer further having a local oscillator input coupling (140), the local oscillator input coupling having an isolation means for isolation from an oscillator (208), the first mixer receiving an isolated high frequency signal from the oscillator.

7. The line interface circuit of claim 1, the second mixer further having a local oscillator input coupling (141), the local oscillator input coupling receiving a high frequency signal from an oscillator (208).

8. A line interface circuit (100) coupling data terminal equipment with a line, the line having a data signal, comprising:

(a) a mixer (102) coupled to the line for receiving the data signal, the mixer having a means for transforming the data signal to a high frequency data signal (110);

(b) a isolation means for isolating the high frequency data signal from the line, the means for isolating being coupled to the mixer, the means for isolating thereby generating an isolated high frequency data signal; and,

(c) a conversion means for converting the isolated high frequency data signal to an isolated low frequency data signal, the means for converting being coupled to isolation means.

9. The line interface circuit of claim 8, where the isolation means comprises high voltage capacitors (105) connected between the mixer and the conversion means.

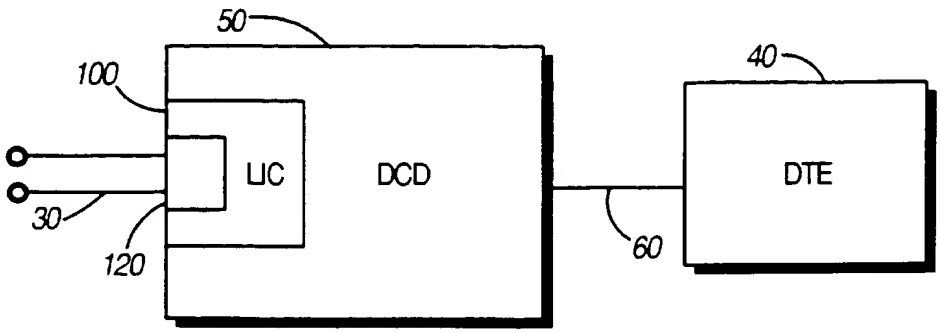

FIG.1

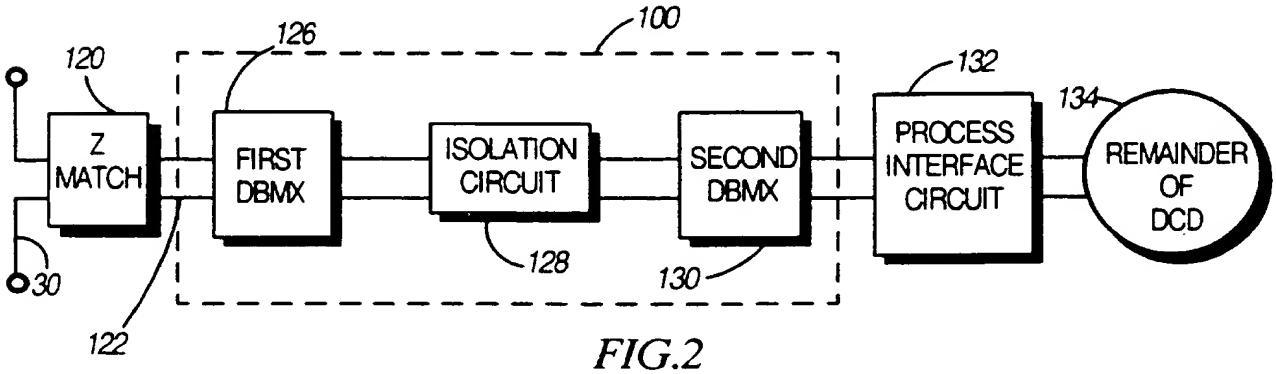

FIG.2

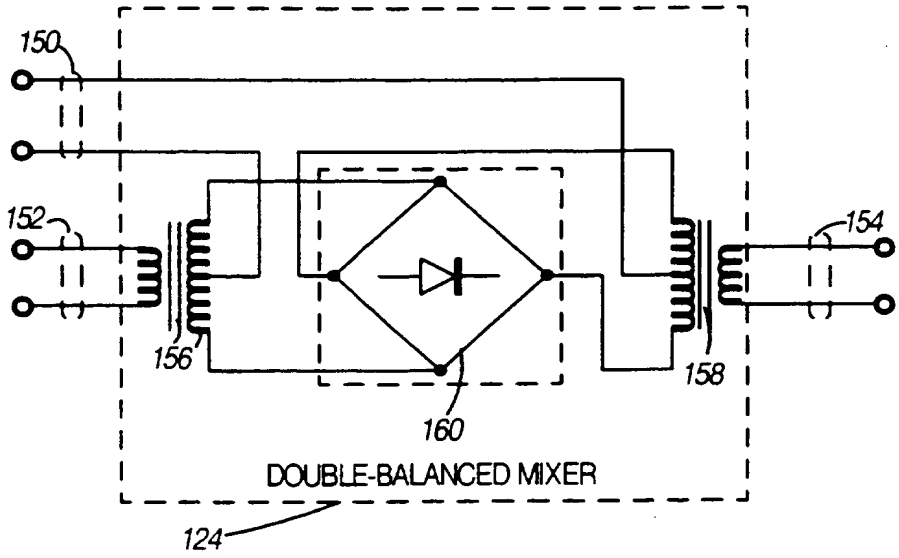

FIG.3

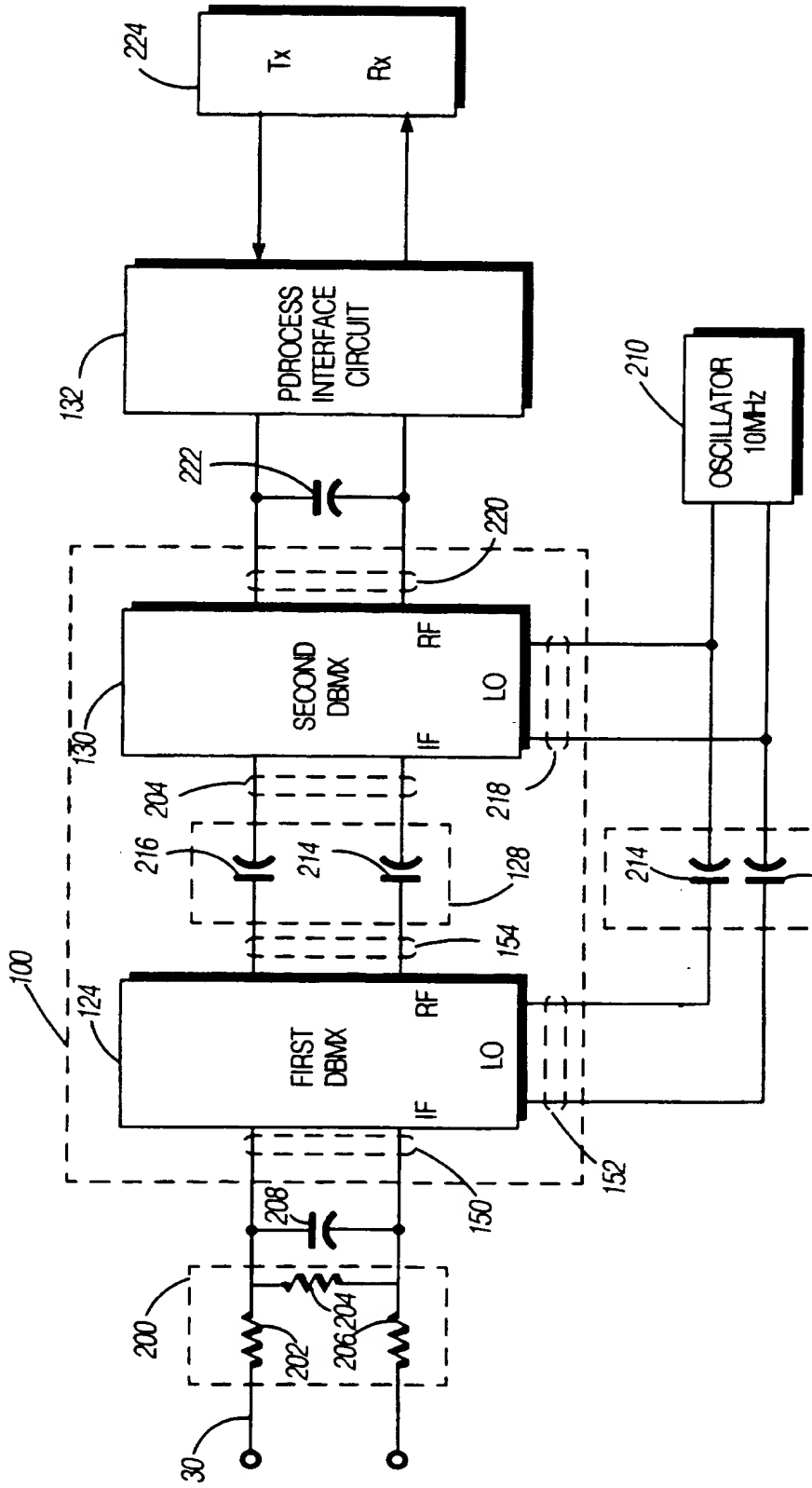

FIG.4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/06516

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H04B 1/38
US CL : 375/220
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/220,219,257; 379/298, 399, 401

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, DIALOG
search terms: line interface, voltage isolat?, mixer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,536,618 (SERRANO) 20 August 1985, abstract, summary of the invention.	1-12
A	US, A, 4,598,173 (CHEA, JR. et al.) 01 July 1986, abstract, summary of the invention.	1-12

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